



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,940	12/14/2001	Michael J. LaGasse	PHX-0001CIP	1746

7590

01/24/2006

Steven M. Mills  
MILLS & ONELLO, LLP  
Suite 605  
Eleven Beacon Street  
Boston, MA 02108

EXAMINER

LEUNG, WAI LUN

ART UNIT

PAPER NUMBER

2633

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/017,940	LAGASSE ET AL.	
	Examiner	Art Unit	
	Danny Wai Lun Leung	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 September 2002.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-80 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21, 23, 24, 26, 27, 29-35, 38-50, 52, 53, 55, 56, 58-68 and 72-80 is/are rejected.
- 7) ☒ Claim(s) 22, 25, 28, 36, 37, 51, 54, 57 and 69-71 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____  | 6) <input checked="" type="checkbox"/> Other: <u>Sano, Iwatsuki</u>         |

## DETAILED ACTION

### *Priority*

1. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 3, 4, 32, and 33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not disclose expressly wherein the control signal is generated so as to **maximize amplitude** of the recovered clock signal.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 30 and 78 are rejected under 35 U.S.C. 102(b) as being anticipated by “80 Gb/s Optical Soliton Transmissino Over 80km with Time/Polarization Divisio Multiplexing” by K.

Art Unit: 2633

Iwatsuki et al in IEEE Photonics Technology Letters, Vol 5, No. 2, Feb 1993; hereafter refer to as Iwatsuki.

Regarding to claims 30 and 78, Iwatsuki discloses a method with an apparatus for demultiplexing a multiplexed signal, said multiplexed signal being a combination of a plurality of component signals, each component signal being characterized by a polarization (*page 246, col 1, "A 40 Gb/s TDM pulse stream was produced with the fiber-delays. In the following polarization maintaining fiber, the TDM pulses were orthogonally split..."*), said apparatus comprising: an input interface over which the multiplexed signal can be received (*page 246, col 1, "The pulse stream was injected into an 80km transmission line ..." thus the transmission line, inherently acting as an input interface, receives the multiplexed signal*); at least one polarization demultiplexer for receiving the multiplexed signal from the input interface and generating therefrom at least one polarization demultiplexed signal of a first polarization (*page 246, col 2, "The 80Gb/s optical signal was first demultiplexed with a polarization beam splitter (PBS)"*); and a time demultiplexing stage for receiving the at least one polarization demultiplexed signal and time demultiplexing the polarization demultiplexed signal to generate at least one time and polarization demultiplexed signal (*page 246, col 2, "The receiver consisted of an EDFA, two cascaded LN modulators operating as an optical demultiplexer... The 80Gb/s optical signal was first demultiplexed with a polarization beam splitter (PBS)"*).

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1-12, 14-18, 31-35, 38-40, 42-47, and 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over “80 Gb/s Optical Soliton Transmissino Over 80km with Time/Polarization Divisio Multiplexing” by K. Iwatsuki et al in IEEE Photonics Technology Letters, Vol 5, No. 2, Feb 1993; hereafter refer to as Iwatsuki, as applied to claim 30 above, in view of US Patent Number 6,486,990 to Roberts et al.

Regarding to claims 1, 31, and 77, Iwatsuki discloses the method with an apparatus for demultiplexing a multiplexed signal in accordance to claim 30 and 78 as discussed above. Iwatsuki further discloses wherein the apparatus further comprising a clock recovery circuit for receiving the polarization demultiplexed signal and recovering therefrom a recovered clock signal, the recovered clock signal being used to generate a control signal, the control signal being used to adjust a demultiplexer (*page 246, col 2, “The LN modulators were driven with 10 GHz sinusoidal waves of  $2V_{\pi}$  and  $V_{\pi}$  amplitude from a 10 Ghz clock recovery circuit, so as to demultiplex the 40Gb/s pulses to 10Gb/s).* Iwatsuki does not disclose expressly that the demultiplexer being adjusted with the control signal is the polarization demultiplexer. Roberts,

Art Unit: 2633

from the same field of endeavor, teaches a method and apparatus for optical transmission system including receiving a polarization demultiplexed signal and recovering therefrom a recovered clock signal, the recovered clock signal being used to generate a control signal, the control signal being used to adjust the polarization demultiplexer (*col 10, ln 4-18; fig 4, fig 13*). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to use the recovered clock signal from the polarization demultiplexed signal as a control signal as taught by Roberts, to adjust the polarization demultiplexer in Iwatsuki's system. The motivation for doing so would have been to keep the amplitude of the clock signal at a maximum level by having a control signal to control the polarization (*col 10, ln 14-18*).

As to claims 2 and 35, Iwatsuki further discloses wherein the multiplexed signal is characterized by a bit rate (*as stated on page 246, column 2, a multiplexed signal on the optical line is characterized by a bit rate of 80Gb/s, after PBS it is characterized by a bit rate of 40Gb/s, after the first LN modulator it is characterized by a bit rate of 20Gb/s, after the second modulator it is characterized by a bit rate of 10Gb/s, similar to applicant's disclosure on page 3 of the specification*), the recovered clock signal having a frequency of one-half the bit rate (*the recovered clock signal have a frequency of 10Gb/s, half of the bit-rate of the multiplexed signal before the second LN modulator*).

As to claim 3, 4, 32, and 33, Roberts further discloses wherein the control signal is generated so as to maximize amplitude of the recovered clock signal (*col 10, ln 14-18*).

As to claims 5 and 34, Iwatsuki further discloses wherein the control signal is a feedback signal (*as shown in figure 1, page 246, control signal from the 10GHz Clock recovery is feed backed to LN Modulators*).

As to claim 6, Iwatsuki further discloses wherein the multiplexed signal is a cross-polarization multiplexed signal (*on page 6, lines 1-2 of the specification, applicant defines "cross-polarization multiplexed signal" as "adjacent bits within the TDM bit stream have different, e.g. orthogonal, polarizations"; on page 246, col 1 of Iwatsuki, "the TDM pulses were orthogonally split"*).

As to claim 7, Iwatsuki further discloses wherein a first component signal of the multiplexed signal is characterized by a first polarization and a second component signal of the multiplexed signal is characterized by a second polarization different than the first polarization (*page 246, col 1, "the TDM pulses were orthogonally split"*).

As to claims 8-10, 38, 44, and 45, Iwatsuki further discloses wherein the multiplexed signal is a time-division multiplexed (TDM) combination of the component signals, and wherein adjacent component signals within the TDM signal have different polarizations, which are orthogonal polarizations (*page 246, col 1, "the TDM pulses were orthogonally split"*).

As to claims 11 and 39, Iwatsuki further discloses wherein the polarization demultiplexer comprises a polarization beam splitter (*page 246, col 2, "The 80Gb/s optical signal was first demultiplexed with a polarization beam splitter (PBS)"*).

As to claims 12 and 40, Iwatsuki further discloses wherein the polarization demultiplexer comprises a polarization transformer (*according to applicant's cited reference, application 09/881,508, also published as US PGPub 2002/0191265, incorporated by reference as a part of the specification, a polarization transformer receives an optical signal at an input and generates a transformed optical signal at an output, wherein the output optical signal has a polarization state within a predetermined range; Iwatsuki's polarization demultiplexer comprises a*

Art Unit: 2633

*“polarization controller, employed to adjust the pulse stream’s state of polarization”, as described on page 246, column 2, and shown in fig 1, reads on the above description of a polarization transformer.)*

As to claims 14 and 42, Iwatsuki further discloses wherein the polarization demultiplexer generates a pair of polarization demultiplexed signals *(note in fig 1, PBS output a demultiplexed signal to the PIN and a demultiplexed signal to the LN mod.)*

Regarding to claim 15, Iwatsuki further discloses wherein the apparatus as discussed above in accordance to claim 1 further comprises a time demultiplexer *(LN modulators, fig 1)* for receiving the polarization demultiplexed signal and generating therefrom at least one time and polarization demultiplexed signal. *(page 245, col 2, “time-division multiplexing/demultiplexing (TDM) techniques”; page 246, col 1, “A 40 Gb/s TDM pulse stream was produced with the fiber-delays. In the following polarization maintaining fiber, the TDM pulses were orthogonally split...”; page 246, col 2, “The LN modulators where driven with 10 GHz sinusoidal waves of of  $2V_{\pi}$  and  $V_{\pi}$  amplitude from a 10 Ghz clock recovery circuit, so as to demultiplex the 40Gb/s pulses to 10Gb/s.”)*

As to claims 16 and 43, Iwatsuki further discloses wherein the at least one time and polarization demultiplexed signal is a recovered version of one of the component signals *(page 246).*

As to claims 17 and 46, Iwatsuki further discloses wherein the time demultiplexer comprises at least one electro-optical (EO) modulator *(LN modulator, fig 1)* for generating the at least one time and polarization demultiplexed signal. *(page 246, col 2, “The LN modulators*



Art Unit: 2633

*where driven with 10 GHz sinusoidal waves of  $2V_{\pi}$  and  $V_{\pi}$  amplitude from a 10 GHz clock recovery circuit, so as to demultiplex the 40Gb/s pulses to 10Gb/s."*)

As to claims 18 and 47, Iwatsuki further discloses wherein the polarization demultiplexed signal is aligned to the input of the EO modulator (*in fig 1, the polarization demultiplexed signal from the PBS is aligned to the input of the LN modulator*).

9. Claims 13 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over "80 Gb/s Optical Soliton Transmissino Over 80km with Time/Polarization Divisio Multiplexing" by K. Iwatsuki et al in IEEE Photonics Technology Letters, Vol 5, No. 2, Feb 1993; hereafter refer to as Iwatsuki, in view of US Patent Number 6,486,990 to Roberts et al. as applied to claims 12 and 40 above, and further in view of US Patent Number 4,233,576 to Pelchat.

Regarding to claims 13 and 41, the combination of Iwatsuki and Roberts discloses the limitation of claims 12 and 40. It does not disclose expressly wherein the polarization transformer comprises a plurality of cascaded retardation waveplates. Pelchat, from the same field of endeavor, teaches a polarization demultiplexing apparatus including a polarization transformer comprising a plurality of cascaded retardation waveplates (24, 26, 44, and 46, fig 1; *also described in col 4, ln 25-41*). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to use Pelchat's polarization transformer comprising a plurality of cascaded retardation waveplates onto the combination of Iwatsuki and Roberts' system to replace the polarization transformer (*Iwatsuki's polarization controller is a polarization transformer as discussed above regarding claim 12*). The motivation for doing so

Art Unit: 2633

would have been to independently control and transform different polarizations by using cascaded retardation waveplates as a part of the polarization transformer.

10. Claims 19-21, 23, 24, 26, 27, 48-50, 52, 53, 55, and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over “80 Gb/s Optical Soliton Transmissino Over 80km with Time/Polarization Divisio Multiplexing” by K. Iwatsuki et al in IEEE Photonics Technology Letters, Vol 5, No. 2, Feb 1993; hereafter refer to as Iwatsuki, in view of US Patent Number 6,486,990 to Roberts et al. as applied to claims 17 and 46 above, and further in view of US Patent Number 6,118,564 to Ooi et al.

Regarding to claims 19 and 48, the combination of Iwatsuki and Roberts discloses a method and an apparatus in accordance to claims 17 and 46. It does not disclose expressly that the EO modulator is a 1x2 modulator having one input and two outputs. Ooi, from the same field of endeavor, teaches an optical demultiplexing apparatus comprising an EO modulator that is a 1x2 modulator having one input and two outputs (*fig 21*). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to use Ooi’s EO modulator onto the combination of Iwatsuki and Roberts’s demultiplexing system such that the EO modulator is a 1x2 modulator having one input and two outputs as taught by Ooi. The motivation for doing so would have been to clearly distinguish the two demultiplexed outputs by having two outputs from the EO modulator that is a 1x2 modulator.

Regarding to claims 20, 23, 26, 49, 52, and 55, the combination of Iwatsuki and Roberts discloses a method and an apparatus in accordance to claims 17 and 46. Iwatsuki further discloses the EO modulator (*LN mod. as shown in fig 1*) comprises an RF input (*from the bottom,*

Art Unit: 2633

*where the signal from the clock recovery circuit is fed into, as shown in fig 1), and having a clock signal applied to the RF input. The combination of Iwatsuki and Roberts does not disclose expressly having a phase-adjusted version of the recovered clock signal. Ooi, from the same field of endeavor, teaches a demultiplexing apparatus (fig 22) including an EO modulator (22, fig 22) comprising an RF input, and have a phase-adjusted version of the recovered clock signal (“drift detection information based on the difference between the phase...” col 21, ln 47-54;*

*“...applying a bias voltage corresponding to the detected drift in a superposing relationship with a clock signal to be supplied to the optical switch” col 21, ln 39-col 22, ln 5), including a harmonic and a sub-harmonic (fig 6, 23, 27, and 29), being applied to the RF input (from the bottom of 22 as shown in fig 22). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to use Ooi’s modulator onto the combination of Iwatsuki and Roberts’s system such that a phase-adjusted version of the combination of Iwatsuki and Roberts’ recovered clock signal, including a harmonic and a sub-harmonic, is applied to the RF input of the modulator in the combination of Iwatsuki and Roberts’s system as taught by Ooi. The motivation for doing so would have been to a phase-adjusted version of the recovered clock signal, including a harmonic and a sub-harmonic component, being applied to the RF input such that the clock recovered signal can be precisely used to demultiplex the signal.*

As to claims 21, 24, 27, 50, 53, and 56, Iwatsuki further discloses the apparatus as discussed above in accordance to claims 20, 23, 26, 49, 52, and 55 further comprising an error signal generating device (*error detector, fig 1*) for receiving the at least one time and polarization demultiplexed signal (*from decision circuit as shown in fig 1*) and generating an error signal (*inherent property of an error detector*). Ooi further teaches using an error signal to adjust the

Art Unit: 2633

phase of the phase-adjusted version of the recovered clock signal (*"drift detection information based on the difference between the phase..." col 21, ln 47-54; "...applying a bias voltage corresponding to the detected drift in a superposing relationship with a clock signal to be supplied to the optical switch" col 21, ln 39-col 22, ln 5*), including a harmonic and a sub-harmonic component (*fig 6, 23, 27, and 29*). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to used the error signal detected by Iwatsuki's error detector to generate an error signal for adjusting the phase of the phase-adjusted version of the recovered clock signal in the combination of Iwatsuki, Roberts, and Ooi's system, including a harmonic and a sub-harmonic component, as taught by Ooi. The motivation for doing so would have been to precisely demultiplex the signal by using an error signal for adjusting the phase of the phase-adjusted version of the recovered clock signal including a harmonic and a sub-harmonic component.

11. Claims 58, 61-63, and 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over "80 Gb/s Optical Soliton Transmissino Over 80km with Time/Polarization Divisio Multiplexing" by K. Iwatsuki et al in IEEE Photonics Technology Letters, Vol 5, No. 2, Feb 1993; hereafter refer to as Iwatsuki, in view of US Patent Number 5,111,322 to Bergano et al.

Regarding to claims 58 and 79, Iwatsuki discloses a method and an apparatus with the cited limitation as discussed above regarding claim 30, and further discloses wherein the apparatus having each component signal being characterized by a polarization and including a data signal pattern (*page 246, col 2, "Fig. 3(a) and (b) show the eye patterns of the monitored 40 Gb/s pulse stream before and after transmission, respectively"*), further comprising: at least one

Art Unit: 2633

receiver associated with one of a plurality of data signal patterns (*as shown in fig 1*), the receiver analyzing the data signal pattern of a component signal recovered from the multiplexed signal to determine if the data signal pattern matches the data signal pattern associated with the at least one receiver (*page 246, col 2, "The 10Gb/s optical receiver equalized the demultiplexed pulse stream using an electrical low-pass filter (7 GHz bandwidth)"*), the at least one receiver providing a feedback signal indicative of whether the analyzed data signal pattern matches the data signal pattern associated with the at least one receiver, and the feedback signal being used to adjust a demultiplexer if the analyzed data signal pattern does not match the data signal pattern associated with the at least one receiver (*page 246, col 2, "...also extracted the 10 GHz timing clock which was fed to the LN demultiplexer and an error detector."*). Iwatsuki does not disclose expressly having a feedback signal indicative of whether the analyzed data signal pattern matches the data signal pattern associated with the at least one receiver, and the feedback signal being used to adjust the polarization demultiplexer if the analyzed data signal pattern does not match the data signal pattern associated with the at least one receiver. Bergano, from the same field of endeavor, teaches a polarization multiplexing system including a feedback signal (*ERROR SIGNAL, fig 4*) indicative of whether the analyzed data signal pattern matches the data signal pattern associated with the at least one receiver (*408, fig 4*), and the feedback signal being used to adjust the polarization demultiplexer (*402, fig 4*) if the analyzed data signal pattern does not match the data signal pattern associated with the at least one receiver (*col 5, ln 29-43*).

Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to use the error signal in Iwatsuki's system as a feedback signal indicative of whether the analyzed data signal pattern matches the data signal pattern associated with the at least one

Art Unit: 2633

receiver in Iwatsuki's system as taught by Bergano. The motivation for doing so would have been to nulls out the unwanted channel in each receiver (*Bergano, col 5, ln 38-43*).

Regarding to claim 61, Iwatsuki further discloses wherein the apparatus as discussed above in accordance to claim 58 further comprises a time demultiplexer (*LN modulators, fig 1*) for receiving the polarization demultiplexed signal and generating therefrom at least one time and polarization demultiplexed signal. (*page 245, col 2, "time-division multiplexing/demultiplexing (TDM) techniques"; page 246, col 1, "A 40 Gb/s TDM pulse stream was produced with the fiber-delays. In the following polarization maintaining fiber, the TDM pulses were orthogonally split..."; page 246, col 2, "The LN modulators where driven with 10 GHz simusoidal waves of of  $2V_{\pi}$  and  $V_{\pi}$  amplitude from a 10 Ghz clock recovery circuit, so as to demultiplex the 40Gb/s pulses to 10Gb/s."*)

As to claim 62, Iwatsuki further discloses wherein the at least one time and polarization demultiplexed signal is a recovered version of one of the component signals (*page 246*).

As to claim 63, Iwatsuki further discloses wherein the time demultiplexer comprises at least one electro-optical (EO) modulator (*LN modulator, fig 1*) for generating the at least one time and polarization demultiplexed signal. (*page 246, col 2, "The LN modulators where driven with 10 GHz simusoidal waves of of  $2V_{\pi}$  and  $V_{\pi}$  amplitude from a 10 Ghz clock recovery circuit, so as to demultiplex the 40Gb/s pulses to 10Gb/s."*)

12. Claims 60 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over "80 Gb/s Optical Solition Transmissino Over 80km with Time/Polarization Divisio Multiplexing" by K. Iwatsuki et al in IEEE Photonics Technology Letters, Vol 5, No. 2, Feb 1993; hereafter refer

Art Unit: 2633

to as Iwatsuki, in view of US Patent Number 5,111,322 to Bergano et al., as applied to claim 58 and 63 above, and further in view of US Patent Number 6,486,990 to Roberts et al.

Regarding to claims 60 and 64, the combination of Iwatsuki and Bergano discloses the method with an apparatus for demultiplexing a multiplexed signal in accordance to claim 58 as discussed above. Iwatsuki further discloses wherein the apparatus further comprising a clock recovery circuit for receiving the polarization demultiplexed signal and recovering therefrom a recovered clock signal, the recovered clock signal being used to generate a control signal, the control signal being used to adjust a demultiplexer (*page 246, col 2, "The LN modulators were driven with 10 GHz sinusoidal waves of  $2V_{\pi}$  and  $V_{\pi}$  amplitude from a 10 Ghz clock recovery circuit, so as to demultiplex the 40Gb/s pulses to 10Gb/s*). The combination of Iwatsuki and Bergano does not disclose expressly that the demultiplexer being adjusted with the control signal is the polarization demultiplexer. Roberts, from the same field of endeavor, teaches a method and apparatus for optical transmission system including receiving a polarization demultiplexed signal and recovering therefrom a recovered clock signal, the recovered clock signal being used to generate a control signal, the control signal being used to adjust the polarization demultiplexer (*col 10, ln 4-18; fig 4, fig 13*). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to use the recovered clock signal from the polarization demultiplexed signal as a control signal as taught by Roberts, to adjust the polarization demultiplexer in the combination of Iwatsuki and Bergano's system. The motivation for doing so would have been to keep the amplitude of the clock signal at a maximum level by having a control signal to control the polarization (*Roberts col 10, ln 14-18*).

Art Unit: 2633

13. Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over “80 Gb/s Optical Solition Transmissino Over 80km with Time/Polarization Divisio Multiplexing” by K. Iwatsuki et al in IEEE Photonics Technology Letters, Vol 5, No. 2, Feb 1993; hereafter refer to as Iwatsuki, in view of US Patent Number 5,111,322 to Bergano et al., and further in view of US Patent Number 6,486,990 to Roberts et al., as applied to claim 64 above, and further in view of US Patent Number 6,118,564 to Ooi et al.

Regarding to claim 65, the combination of Iwatsuki, Bergano, and Roberts discloses a method and an apparatus in accordance to claim 64. Iwatsuki further discloses the EO modulator (*LN mod. as shown in fig 1*) comprises an RF input (*from the bottom, where the signal from the clock recovery circuit is fed into, as shown in fig 1*), and having a clock signal applied to the RF input. The combination of Iwatsuki, Bergano, and Roberts does not disclose expressly having a phase-adjusted version of the recovered clock signal. Ooi, from the same field of endeavor, teaches a demultiplexing apparatus (*fig 22*) including an EO modulator (*22, fig 22*) comprising an RF input, and have a phase-adjusted version of the recovered clock signal (*“drift detection information based on the difference between the phase...” col 21, ln 47-54; “...applying a bias voltage corresponding to the detected drift in a superposing relationship with a clock signal to be supplied to the optical switch” col 21, ln 39-col 22, ln 5*), including a harmonic and a sub-harmonic (*fig 6, 23, 27, and 29*), being applied to the RF input (*from the bottom of 22 as shown in fig 22*). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to use Ooi’s modulator onto the combination of Iwatsuki, Bergano, and Roberts’ system such that a phase-adjusted version of Iwatsuki’s recovered clock signal, may include a harmonic and a sub-harmonic as taught by Ooi, is applied to the RF input of the



Art Unit: 2633

modulator in Iwatsuki's system as taught by Ooi. The motivation for doing so would have been to a phase-adjusted version of the recovered clock signal, including a harmonic and a sub-harmonic component, being applied to the RF input such that the clock recovered signal can be precisely used to demultiplex the signal.

14. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over "80 Gb/s Optical Soliton Transmissino Over 80km with Time/Polarization Divisio Multiplexing" by K. Iwatsuki et al in IEEE Photonics Technology Letters, Vol 5, No. 2, Feb 1993; hereafter refer to as Iwatsuki, in view of US Patent Number 5,111,322 to Bergano et al., as applied to claim 58 above, and further in view of US Patent Number 4,233,576 to Pelchat.

Regarding to claim 59, the combination of Iwatsuki and Bergano discloses the limitation of claim 58. It does not disclose expressly wherein the adjustment of the polarization demultiplexer if the analyzed data signal pattern does not match the data signal pattern associated with the at least one receiver includes rotating the polarization of the at least one polarization demultiplexed signal to an orthogonal state. Pelchat, from the same field of endeavor, teaches wherein wherein the adjustment of the polarization demultiplexer if the analyzed data signal pattern does not match the data signal pattern associated with the at least one receiver includes rotating the polarization of the at least one polarization demultiplexed signal to an orthogonal state (*col 3, ln 21-52*). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to use Pelchat's polarization transformer to replace the combination of Iwatsuki and Bergano's polarization transformer such that the adjustment of the polarization demultiplexer includes rotating the polarization of the at least one polarization demultiplexed

Art Unit: 2633

signal to an orthogonal state if the analyzed data signal pattern does not match the data signal pattern associated with the at least one receiver. The motivation for doing so would have been to independently adjust different polarizations by rotating the polarization of the at least one polarization demultiplexed signal to an orthogonal state in order to establish a sufficiently precise polarization discrimination system (*Pelchat, col 1, ln 15-19*).

15. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over “80 Gb/s Optical Soliton Transmissino Over 80km with Time/Polarization Divisio Multiplexing” by K. Iwatsuki et al in IEEE Photonics Technology Letters, Vol 5, No. 2, Feb 1993; hereafter refer to as Iwatsuki, in view of US Patent Number 5,111,322 to Bergano et al., and further in view of US Patent Number 6,486,990 to Roberts et al., and further in view of US Patent Number 6,118,564 to Ooi et al. as applied to claim 65 above, and further in view of US Patent Number 4,233,576 to Pelchat.

Regarding to claim 66, the combination of Iwatsuki, Bergano, Roberts, and Ooi discloses the apparatus as discussed above in accordance to claim 65. It does not disclose expressly that if the analyzed data signal pattern does not match the data signal pattern associated with the at least one receiver, the phase of the clock signal applied to the RF input is adjusted 180 degrees.

Pelchat, from the same field of endeavor, teaches a phase shift of 180 degrees if the analyzed data signal pattern does not match a predetermined data signal pattern (*col 3, ln 37-52*).

Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to apply Pelchat’s teaching onto the combination of Iwatsuki, Bergano, Roberts, and Ooi’s system such that if the analyzed data signal pattern does not match the data signal pattern

Art Unit: 2633

associated with the at least one receiver in the combination of Iwatsuki, Bergano, Roberts, and Ooi's system, the phase of the clock signal applied to the RF input is adjusted 180 degrees as taught by Pelchat. The motivation for doing so would have been to be able to precisely demultiplex a polarized signal with the original phase and polarization components recovered.

16. Claims 67, 68, 72-74, and 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over "80 Gb/s Optical Soliton Transmissino Over 80km with Time/Polarization Divisio Multiplexing" by K. Iwatsuki et al in IEEE Photonics Technology Letters, Vol 5, No. 2, Feb 1993; hereafter refer to as Iwatsuki, in view of US Patent Number 5,111,322 to Bergano et al., as applied to claim 64 above, and further in view of US Patent Number 6,118,564 to Ooi et al.

Regarding to claims 67 and 80, Iwatsuki discloses an apparatus for demultiplexing a multiplexed signal, said multiplexed signal being a combination of a plurality of component signals, each component signal being characterized by a polarization (*page 246, col 1, "A 40 Gb/x TDM pulse stream was produced with the fiber-delays. In the following polarization maintaining fiber, the TDM pulses were orthogonally split..."*), said apparatus comprising: an input interface over which the multiplexed signal can be received (*page 246, col 1, "The pulse stream was injected into an 80km transmission line ..." thus the transmission line, inherently acting as an input interface, receiving the multiplexed signal*); a clock recovery circuit for receiving the multiplexed signal and recovering therefrom a clock signal (*page 246, col 2, "The LN modulators were driven with 10 GHz sinusoidal waves of  $2V_{\pi}$  and  $V_{\pi}$  amplitude from a 10 Ghz clock recovery circuit, so as to demultiplex the 40Gb/s pulses to 10Gb/s*); an electro-optical modulator (*LN modulator mentioned above*) for receiving the multiplexed signal and generating

Art Unit: 2633

at least one demultiplexed signal therefrom (*page 246, col 2, "... so as to demultiplex the 40Gb/s pulses to 10Gb/s*), the electro-optical modulator including an RF input and a bias input, the RF input receiving a phase-adjusted version of the clock signal (*page 246, col 2, "The LN modulators were driven with 10 GHz sinusoidal waves of  $2V_{\pi}$  and  $V_{\pi}$  amplitude from a 10 GHz clock recovery circuit...*" as an RF signal, and the output of the PBS as a bias input); a detector circuit for detecting the at least one demultiplexed signal from the electro-optical modulator and generating therefrom an error signal (*"Error detector" fig 1*); Iwatsuki does not disclose expressly that the apparatus comprising a processor for receiving the error signal from the detector circuit and generating a control signal based on the error signal, the control signal being used to adjust the phase of the clock signal applied to the RF input of the electro-optical modulator. Bergano, from the same field of endeavor, teaches a polarization demultiplexing apparatus (*fig 4*) comprising a processor (*402, fig 4*) for receiving the error signal from the detector circuit (*410, fig 4*) and generating a control signal based on the error signal (*col 5, ln 31-43*). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to include a processor as taught by Bergano, onto Iwatsuki's system such that the error signal on Iwatsuki's system can be used by the processor to generate a control signal. The motivation for doing so would have been to stabilize the system by having a processor to generate a control signal based on the error signal.

The combination of Iwatsuki and Bergano does not disclose expressly wherein the control signal is being used to adjust the phase of the clock signal applied to the RF input of the electro-optical modulator. Ooi, from the same field of endeavor, teaches an optical time division demultiplexing apparatus which comprise a control signal based on an error signal

*("drift detection information based on the difference between the phase..." col 21, ln 47-54)*

being used to adjust the phase of a clock signal (*"...applying a bias voltage corresponding to the detected drift in a superposing relationship with a clock signal to be supplied to the optical switch" col 21, ln 39-col 22, ln 5*) applied to an RF input of an electro-optical modulator (22, fig 7). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to use the control signal of the combination of Iwatsuki and Bergano to adjust the phase of the clock signal applied to the RF input of the electro-optical modulator in the system of the combination of Iwatsuki and Bergano as taught by Ooi. The motivation for doing so would have been to stabilize the operating point of the system by controlling the phase of the clock signal based on the error control signal (*Ooi, col 22, ln 17-31*).

As to claim 68, Iwatsuki further discloses wherein the error signal is a signal having a frequency equal to a data rate of the demultiplexed signal (*note in fig 1, error detector and LN modulators are both driven by the clock recovery signal to provide error signal and data signal respectively, thus the error signal and data signal should have the same frequency*).

As to claim 72, the combination of Iwatsuki, Bergano, and Ooi disclose the apparatus as discussed above in accordance to claim 67, Ooi further discloses wherein the control signal is generated to adjust the phase of the clock signal, as discussed above regarding claim 67, to optimize an attribute of the demultiplexed signal (*col 24, ln 19-38, "while compensating for an operating point drift and consequently a demultiplexed signal having a sufficient optical output intensity can be outputted."*)

As to claim 73, Ooi further discloses wherein the attribute is optical intensity of the demultiplexed signal (*col 24, ln 19-38*). Ooi does not disclose expressly wherein the attribute is

Art Unit: 2633

error rate in the demultiplexed signal. Iwatsuki, from the same field of endeavor, further discloses the bit-error-rate (BER) is a function of averaged received power, or intensity (*page 246, col 2, also shown in fig 4*). Therefore it would have been obvious for a person of ordinary skill in the art at the time of invention to view the optical intensity of Ooi's teaching as an error rate attribute as taught by Iwatsuki. The motivation for doing so would have been to be able to measure error rate based on a physical attribute such as optical intensity.

As to claim 74, Iwatsuki further discloses wherein the optimization is done (*page 246, col 2 "No error-rate floor was observed." with low bit error rate and noise accumulation as described in the 2<sup>nd</sup> paragraph of col2*) by decoding information in the demultiplexed signal (*page 246, col 2, "... equalized the demultiplexed pulse stream using an electrical low-pass filter..., and also extracted the 10 GHz timing clock which was fed to the LN demultiplexer and an error detector"*).

17. Claim 75 and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over "80 Gb/s Optical Soliton Transmissino Over 80km with Time/Polarization Divisio Multiplexing" by K. Iwatsuki et al in IEEE Photonics Technology Letters, Vol 5, No. 2, Feb 1993; hereafter refer to as Iwatsuki, in view of US Patent Number 5,111,322 to Bergano et al., and further in view of US Patent Number 6,118,564 to Ooi et al., as applied to claim 74 above, and further in view of US Patent Number 6,941,078 to Onaka.

Regarding claims 75 and 76, the combination of Iwatsuki, Bergano, and Ooi discloses the limitation as discussed above in accordance to claim 74. Iwatsuki further discloses wherein the decoded information includes clock signal. The combination does not disclose expressly that the

Art Unit: 2633

clock signal is an error correction information or forward error correction (FEC) information.

Onaka, from the same field of endeavor, teaches that a recovered clock signal can be used to make forward error correction (FEC) signal, a type of error correction information (*col 1, ln 40-43; col 2, ln 7-9*). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to treat Iwatsuki's clock signal recovered from the decoding information in the demultiplexed signal in the combination of Iwatsuki, Bergano, and Ooi system as a forward error correction (FEC) signal, a type of error correction information, as taught by Onaka. The motivation for doing so would have been to provide an improved method and system for communicating a multiplexed signal over an optical link.

#### ***Allowable Subject Matter***

18. Claims 22, 25, 28, 29, 36, 37, 51, 54, 57, and 69-71 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

#### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Wai Lun Leung whose telephone number is (571) 272-5504. The examiner can normally be reached on 9am-6:30pm Mon-Thurs, except federal holidays.

Art Unit: 2633

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DWL  
January 11, 2006

  
JASON CHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600